Channel Encoding Block for Mobile WiMAX Networks Using Reconfigurable Hardware

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Abstract: WiMAX technology aims to provide wireless metropolitan area transmissions with guaranteed quality of service. Towards this aim, sophisticated channel encoding techniques must be implemented in a hardware, which is optimized for such techniques. In this context, this article presents the design of a channel encoder for mobile WiMAX networks, which is prototyped in reconfigurable hardware architecture. The validation of the prototype was conducted considering scheduled traffic in the medium access control layer. Results showed that the channel encoder is fundamental for guaranteeing quality of service in mobile WiMAX networks.

Keywords: Channel Encoding Block, Reconfigurable Hardware, WiMAX.

Introduction

Wireless systems provide support to triple play services, *i.e.* these systems are able to offer integrated transmission for data, voice, and video. An example of wireless system that serves these types of services is the IEEE 802.16 standard (IEEE, 2009). This standard offers broadband access in metropolitan environments with fast deployment, high scalability level, as well as low costs of the maintenance and upgrade (Papapanagiotou *et al.*, 2009). The IEEE 802.16 standard, also known as Worldwide Interoperability for Microwave Access (WiMAX), due to name of the device factory forum for this standard, supports a large amount of applications that demand high traffic capacity and *Quality of Service* (QoS). Examples of these applications are: return channel for digital television system, Video on Demand (VoD), and on-line games, among others.

In wireless systems, the QoS is affected by the time-varying conditions of the transmission medium, caused by several problems related to physical impairments, such as: delay scattering, due to multipath fading, fading, and Doppler effect. These impairments directly influence the transmission quality, since they may generate errors in the transmitted information. To deal with these problems, it is fundamental to optimize the transmission channel capacity in order to guarantee QoS of triple play applications. An important aspect to optimize the transmission channel is to provide error control techniques in the receiver, applying a technique called *Forward Error-Correction* (FEC). Another possibility is the transmission of variable amounts of bits per modulation symbols. In the IEEE 802.16 standard, the modulation type and the FEC encoding rate form a burst profile, which can be dynamically adapted according to the transmission channel conditions (Ko *et al.*, 2010). This mechanism, know as Modulation and Coding Scheme(MCS), when associated with the Orthogonal Frequency Division Multiple Access (OFDMA) multiplexing technique forms the physical interface for the mobile WiMAX networks.

In the recent past, the industry has focused on the developmentof chipsets for mobile WiMAX with support to OFDMA as mandatory physical interface (da Silva *et al.*, 2008). This development usually is based on the design of chipsets using *Application Specific Integrated Circuit* (ASIC), which increases the total cost of the prototype and only allows limited adaptations to technological innovations or enhancements. However, it is also possible to

develop mobile WiMAX devices using reconfigurable hardware. This solution decreases the cost, guarantees good performance, fast development, and the best time-to-market, *i.e.* arrival time of product in the market. In this context, several papers published in the literature were proposed on the channel encoding subject for WiMAX networks (Upadhyaya *et al.*, 2010; Shaker *et al.*, 2010; Elwazeer, *et al.*, 2009) using reconfigurable hardware, for example the prototype in *Field-programmable Gate Array* (FPGA).

The majority of the works regarding to mobile WiMAX prototyped in FPGA are focused on the development of specific modules for the channel encoding defined by the IEEE 802.16 standard. Moreover, to the best of our knowledge, no work considers the scheduled traffic by the *Medium Access Control* (MAC) layer in the evaluation of the developed prototype. Therefore, this article presents two main contributions for the project of a mobile WiMAX device prototyped in FPGA: (i) development of a channel encoding block, with emphasis in the FEC encoding, as well as the usage of OFDMA as multiplexing technique, and (ii) performance evaluation of the prototype considering the traffic scheduled by the MAC layer. The obtained results show that the usage of a channel encoding block is fundamental to guarantee QoS in IEEE 802.16 networks, since it allows the correction of errors during the transmission, what reduces the probability of affecting the overall network QoS.

The remaining of the paper is organized as follows. In Section 2, the background on channel encoding mechanism for IEEE 802.16 networks, as well as the related work is described. In Section 3, the prototyping of the channel coding in a FPGA platform is presented. In Section 4, the obtained results are discussed and, finally in Section 5, the conclusions and future work are presented.

Background

This section aims to present the channel encoding mechanism of mobile WiMAXnetworks. Moreover, the related work about this mechanism, which has been prototyped in the reconfigurable hardware, is discussed.

Chanel Coding Mechanism

The main function of the channel encoding mechanism is to provide reliable transmissions through a Radio Frequency (RF) channel. This mechanism can be seen as a sequential process in mobile WiMAX networks, where the bits before being sent are scrambled, encoded, interleaved, modulated, and finally multiplexed using the OFDMA technique. Figure 1 presents a view of the components of the channel encoding mechanism for the IEEE 802.16 standard, highlighting the phases of FEC encoding, interleaving, and RF channel multiplexing.

The channel encoding process starts with the scrambler, which aims to homogeneously distribute bits that will be sent in the frequency domain. This distribution decreases the power peak, reducing as a result the probability of interference between adjacent subcarriers (Wang, *et al.*, 2008). After the scrambling, the bits are encoded using FEC techniques. In this phase, redundant information is inserted to allow error detection and correction by the receiver device. FEC technique in WiMAX networks is obtained using algorithms as Reed-Solomon (RS), Convolutional Codes (CC), Convolutional Turbo Codes (CTC), or Low-Density Parity Check Codes (LDPC) (Salmon and Olivier, 2007). In the context of Mobile WiMAX, FEC encoding is simply based on the deployment of one encoder, *i.e.* the IEEE 802.16 standard defines the implementation CC as mandatory, while other algorithms are optional.

The application of the encoding technique in the isolated manner is usually not sufficient to efficiently recover from bit errors, especially when the RF channel is affected by bursts of errors. Therefore, FEC encoding is integrated with the interleaving technique that is based on the re-sequence of a block of bits before the transmission occurs. In this technique, originally a distance that may change over time separates adjacent bits. This distance allows more efficient error correction (Shi, *et al.*, 2004).

After the interleaving, bits must be mapped inside a modulation constellation formed by modulation symbols. This process defines the amount of data that shall be transmitted. The mobile WiMAX standard allows the usage of Quadrature Amplitude Modulation (QAM) constellation, turning possible to vary the amount of bits per modulation symbol. The combination of a modulation constellation with a FEC encoding rate defines the MCS. The MCS configuration can be changed dynamically to adapt the reliability of a transmission according to the RF channel propa-
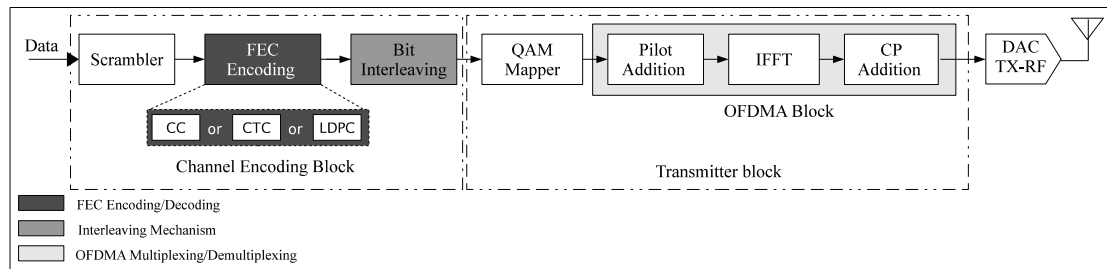
Figure 1. Channel encoding process in Mobile WiMAX.

Table 1. MCS configuration for OFDMA.

Modulation	Bits per Symbols	Convolution Code Rate
BPSK	1	1/2
QPSK	2	1/2
QPSK	2	3/4
16 QAM	4	1/2
16 QAM	4	3/4
64 QAM	6	1/2
64 QAM	6	2/3
64 QAM	6	3/4

gation conditions. Eight MCS configurations are considered in this work, following the IEEE 802.16 recommendation (IEEE, 2009). These configurations, as well as the amount of bits per modulation symbol are presented in Table 1.

The mapped symbols are sent to the OFD-MA block, which is mandatory for the mobile WiMAX standard. The OFDMA multiplexing involves three phases: (i) insertion of pilot subcarriers, to provide synchronization, (ii) the QAM symbols in frequency domain are submitted to Inverse Fast Fourier Transform (IFFT), that converts the signal to the time domain, forming Orthogonal Frequency-Division Multiplexing (OFDM) symbols, and (iii) a guard interval, called Cyclic Prefix (CP), is inserted in the beginning of each OFDM symbol. After the channel encoding, the digital information is passed through a Digital to Analogue Converter (DAC) resulting in an analogical signal, to be transmitted in the RF channel.

Each of the previously described processes is designed in specific modules when prototyped in reconfigurable hardware. In this context, the next subsection presents some related work found in the literature about the usage of a channel encoding block deployment in reconfigurable hardware for the IEEE 802.16 standard.

Related Work

Shaker *et al.* (2010) describe that a FPGA platform is a good option in reconfigurable hardware for deployment of sophisticated signal processing in Software Defined Radios (SDRs). For example, in WiMAX networks, Convolutional Codes are used for encoding and Viterbi algorithm is implemented in the decoding process. Upadhyaya *et al.* (2010) presented a work that used a FPGA platform, where a finite state machine was used to model the interleaving technique. The prototyping of this technique used flip-flops with negligible loss of logical cells, offering the best performance with maximum frequency of transmission. Elwazeer *et al.* (2009) used a FPGA platform to estimate the mobile WiMAX RF channel considering OFDM multiplexing. The deployed solution minimizes the complexity of the RF channel estimate using the Minimum Mean-Square Error (MMSE) technique.

The state of the art about channel encoding process in reconfigurable hardware presents some works that propose specific modules (da Silva *et al.*, 2008). However, the deployment of a prototype that considers all encoding blocks of the physical layer and the traffic scheduled in the MAC layer must be analyzed. This integration between the encoder and the scheduler is fundamental for the per-

formance of a mobile WiMAX device, because the physical layer must guarantee higher traffic transmission rate. In the next section, we present the proposal of a channel encoding block that receives data from the MAC layer.

Channel Encoding Block Prototype

The development of a channel encoding block implemented in a hardware description language allows the analysis of the different communication methods between the MAC layer and the physical layer. Moreover, this development provides a tool evaluate the performance of the channel encoding mechanism when used in a physical device, for example a FPGA representing real operating equipment.

The model used to develop the prototype was designed as shown in Figure 2, which presents in a generic way, the architecture proposal for the channel encoding. In the figure it is possible to observe a module which is responsible for system control, which receives two input signals. The first signal indicates how many Information Elements (IEs) were scheduled in the MAC layer. The other signal specifies the MSC of each burst inside each frame. This module is implemented using a finite state machine, *i.e.* a structure used for both controlling the system operation and the decision-making in hardware level implementations.

The controller module is responsible for generating command signals for all the architecture blocks, guaranteeing the synchronization of the circuit and the integrated operation of the blocks. The module is composed of seven independent state machines that work in a sequential way from the first stage of the encoding until the last stage. Each state machine has a waiting state and one or more operation state. The condition to change from the waiting state to the operation state is analyzed by the state machine corresponding to the previous state. This module is not defined by the IEEE 802.16 standard, therefore the controller

proposal is one of the contributions of this article, designed to be the central point of the proposed architecture, since it feeds the channel encoding process modules with information which allow the execution of such a process.

The channel encoding block receives data from the MAC layer as input. This data is associated with burst profiles that compose an OFDMA frame. In order to obtain these bursts, the MAC layer was simulated with a tool developed using Labview and Matlab software. The parameters used for creating the evaluation methodology follow the definitions presented by the WiMAX forum (WiMAX Forum, 2008). The data signal, after encoded and modulated, generates bits that will be transmitted by the physical interface.

After receiving these three input signals, the architecture must be able to be adapted to perform the codification according to the input data block size. We used this method to input data because it optimizes the division of the blocks that are going to be encoded. Moreover, the interleaving module needs to know the block size that will be used. This information is derived from data received as input into the architecture. The block size value defines the quantity of data bits that will be forwarded to the channel encoding mechanism in each execution cycle. If the amount of input bits is not sufficient to complete the block size, padding must be inserted, using OxFF signal pattern.

To control the different input block sizes, we implemented a module that is responsible for the integration between the MAC and physical layers. This module splits the data stream sent from MAC layer insmaller pieces, corresponding to the channel encoding block size. The block size depends on the amount of allocated data (amount of used resources used in an OFDMA frame), as well as on the MCS used. Moreover, the blocks can be concatenated to improve the system performance.

The remaining modules of the architecture modules were implemented according to the specification of the IEEE 802.16 standard. The last phase of the development was to perform tests considering the integrated system. Therefore, a test module was developed. This module reads data provided by an external file, generates input stimuli to the circuit, and stores the results in an output file. The test module was essential for obtaining and analyzing the results that are presented and discussed in the next section.
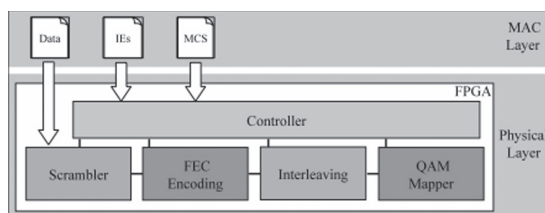

Figure 2. Proposed architecture.

Performance Evaluation

This section describes the performance analysis of the proposed architecture, which was implemented in a FPGA platform. The VoIP and HTTP traffic models were used to represent two common applications typically found in mobile WiMAX networks. These models and the physical configuration of the simulation scenario were based on the System Evaluation Methodology document published by the WiMAX Forum (WiMAX Forum, 2008). Moreover, the functional verification of the channel encoding mechanism was performed using the test vector indicated by the IEEE 802.16 standard (QPSK 1/2 MCS configuration) (IEEE, 2009). Furthermore, all the results were obtained considering a confidence interval of 95%.

The first analysis refers to the number of cyclesin relation to the block size that can be processed by the channel encoding mechanism. According to the IEEE 802.16 standard, the data blocks can be concatenated to improve the system performance. In this way, we understand that the concatenation must be performed with the highest size for each MCS. Thus, to evaluate the performance of this characteristic defined by the standard, we performed an analysis with all possible block sizes for each MCS considering VoIP and HTTP traffics, respectively. Figure 3 presents three burst sizes, using: the highest value (3696 bits), the smallest value (1857 bits), and the average value (2688 bits). Due to the limitation of space in this article, only the MCS configuration 1 was used in this visualization.

We observe that considering the burst sizes of 2688 bits and 1857 the concatenation of blocks increased the circuit performance if compared with a block where no concatenation is applied. However, when the concatenation is performed with the highest possible block size, the circuit presents the worst performance. Analysing the results, we can conclude that the method specified by the standard is not able to attain the best efficiency of the designed circuit. The best performance found in this analysis was obtained using a block size equal to 144, where the circuit used 7542 cycles to encode the data. The same block size leaded to the best performance considering a burst of size equal to 1857 bits, using 5160 cycles for the data processing.

The second analysis of this article investigates the variability caused in the channel encoding output bits. This variability is resultant from the application of the interleaving module. This functionality is fundamental to guarantee the homogeneity of the spectrum, i.e. the balancing between bits with value equal to 0 and 1. In this work, we analyze different initial states for the channel encoding block, which can cause discrepancies among the amount of zeros and ones in the encoding output. The analysis was performed consideringthe random values indicated in Table 2. Moreover, in order to allow a comparison, we also implement the method defined by the IEEE 802.16 standard (IEEE, 2009) to vary the output bits. This method was (N) and its behavior can be observed in Figure 4.

The initialization of the encoding block with predefined values, as can be seen in Table 2, improves the circuit performance, because it is not necessary to developa structure to store data between Interleaving and FEC Encoding. Figure 4 presents the variability of output bits in the channel encoding block. The results present the amount of bits with value equal to 0 and the amount of bits with value
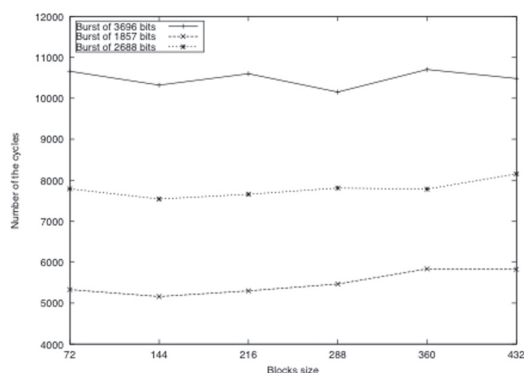

Figure 3. Encoding block using QPSK ½ MCS.

Table 2. MCS representation

Representation	Initial State
BPSK 1/2 (A)	000000
QPSK 1/2 (B)	000111
QPSK 3/4 (C)	001100
16 QAM 1/2 (D)	010101
16 QAM 3/4 (E)	101010
64 QAM 1/2 (F)	110011
64 QAM 2/3 (G)	111000
64 QAM 3/4 (H)	111111
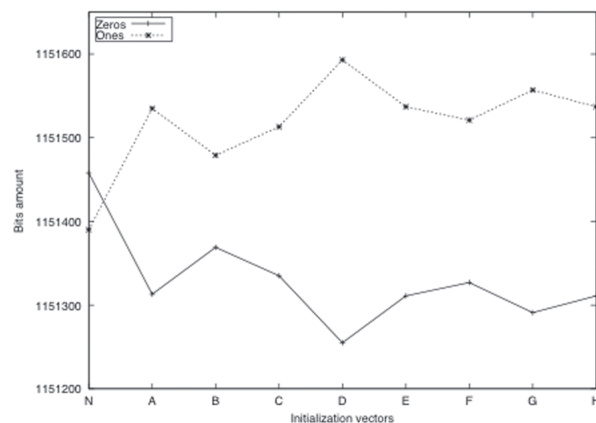
Figure 4. Variability of the encoding process.

Table 3. FPGA used resources

Resources	Available	Used	Percentage Used
Slices	13696	6783	49%
Flip-flops	27392	2484	9%
LUTs	27392	10365	37%
I/Os	556	94	16%

equal to 1. In this analysis, the traffics were also scheduled by the MAC layer.

Analyzing Figure 4, we can observe that the obtained results are close to those obtained with the method proposed by IEEE 802.16 standard. In this analysis, we can highlight the behavior of MCS configuration QPSK 1/2 (B), which presented the best performance among the pre-configured values. Further analysis showed that the standard suggested method was the only one to generate more bits with value equal to one than with value equal to zero. This behavior is justified because the input method of the standard is dynamic. In each cycle the channel encoder is configured with a different MCS configuration. We can conclude from this second analysis that the results obtained considering pre-configured values are close to those obtained with me IEEE 802.16 method. However, we have obtained these results through the application of a programmable logic, which is optimized for this specific functionality. Therefore, our approach demands less computational resources than the IEEE 802.16 suggestion. In this context, the following analysis considers the FPGA resources usage.

A Xilinx Virtex-II Pro FPGA was used for prototyping the channel encoding mechanism, which is not a very powerful model. We used the Integrated Software Environment (ISE) for implementing the synthesis. The main results obtained from the circuit synthesis are related to the resources usage. These results are presented in Table 3. We can observe that the developed circuit used approximately 50% of the most important FPGA resources, i.e. Look Up Tables (LUTs) and Slices.

Another obtained result regards to the maximum operation frequency of the circuit, which was obtained using the tool after the synthesis. The developed circuit is able to operate a maximum frequency close to 180 MHZ. This result shows that the designed circuit is able to proceed with the channel encoding process faster than the specification of IEEE 802.16 standard. In other words, the proposed circuit is able to transmit data frames in less than 5ms, which is the limit imposed by the standard.

Conclusion and Future Work

The main contribution of this article was the design and implementation of a channel encoder prototype using FPGA. Our approach was to emphasize the FEC encoding, as well as the OFDMA multiplexing technique in mobile WiMAX networks. Another contribution regards to the evaluation of the proposed pro-

totype considering the traffic scheduled by the MAC layer, based on traffic models that followed the WiMAX Forum specification. The obtained results showed that the deployment of a channel encoding mechanism is fundamental to guarantee QoS in the context of mobile WiMAX networks.

Directions for future work may involve the implementation of both modulation and channel multiplexing in hardware, in order to allow the performance analysis of the whole transmission cycle. This proposed approach may lead to a more comprehensive analysis of the physical layer of IEEE 802.16 devices.

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