Practical stability analysis of frequency controlled dimmable ballasts

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Resumo

Reatores eletrônicos para alimentação de lâmpadas fluorescentes (LF) vêm substituindo os eletromagnéticos por terem trazido vários benefícios, tais como: (1) ausência de *flicker,* ruído sonoro e efeito estroboscópico; (2) menor tamanho e peso; (3) aumento de fluxo luminoso da LF; (4) redução do consumo de energia elétrica. Além disso, os reatores eletrônicos dimerizáveis possibilitam uma economia de energia elétrica ainda maior e proporcionam um maior conforto ambiental. A dimerização da LF, através da variação da freqüência de comutação dos interruptores do inversor, até 30% da sua potência nominal, geralmente pode ser implementada em malha fechada. Dimerização até os níveis mais baixos de potência somente pode ser atingida sob controle em malha fechada. O artigo apresenta um método prático da análise de estabilidade do conjunto LF - reator eletrônico e descreve o projeto do compensador. A análise teórica é verificada experimentalmente num protótipo de reator eletrônico dimerizável para uma LF modelo T8 de 32 W.

Palavras-chave: iluminação fluorescente, eletrônica de potência, reator eletrônico, dimerização, estabilidade.

Abstract

Electronic ballasts for fluorescent lamps (FL) substitute the electromagnetic ones due to some advantages, such as: (1) no flicker, audible noise or stroboscopic effect; (2) light weight and small size; (3) higher FL light output; (4) reducing of electric power consumption. Moreover, the dimmable electronic ballasts make possible to cut even more the energy consumption and to offer more lighting comfort. The switching frequency dimming until 30% of the rated FL power generally can be implemented under open loop control scheme, while a wider dimming range requires the closed-loop one. The paper presents a practical method for FL – ballast stability analysis and describes a compensator design method. The theoretic analysis is verified experimentally on the dimmable ballast prototype designed to feed one T8 32 W FL.

Key words: *fluorescent lighting, power electronics, electronic ballast, dimming, stability.*

1. Introduction

High-frequency electronic ballasts are widely used to drive FL for improving light quality, reducing power consumption, being light and smaller, eliminating audible noise and stroboscopic effect (Hummer, 1987), (Hummer and Mcgowan, 1985). Additionally, electronic ballasts provide dimming capability which permits to reduce even more the electric power consumption and adjust the lamp light output to the user requirements. Usually, dimmable electronic ballast (DEB) includes a PFC stage and a frequency inverter one, however single-stage integration is possible (Wu *et al.*, 1998).

Basically, there are four dimming methods: (1) variation of the inverter switching frequency (DIM_F); (2) variation of the bus DC voltage (DIM_V); (3) variation of the inverter duty cycle (DIM_D) and (4) switching one of the resonant tank capacitors (DIM_C). Actually, some combinations of these methods can be implemented.

Dimming by DIM_F is the most frequently used method due to the simplicity of implementation (Moo *et al.*, 1999), however the efficiency is low at lower levels of dimming. Dimming by DIM_V provides high efficiency in the whole dimming range (Ho *et al.*, 2001), but the circuit is complex because the input stage includes a PFC and a voltage regulator. Dimming by DIM_D has two drawbacks: (1) when $D<0.23$ the half bridge inverter switches loose soft switching; (2) for $D<0.4$ the non linear electrophoresis phenomenon occurs resulting in light output extinguishing at one of the FL extremities (Raizer, 2002). Dimming by DIM_C is a relatively new dimming method, introduced in Chiu *et al.* (2005), however presents the non linear electrophoresis problem. Taking in consideration the presented argumentations, only the DIM_F is analyzed in the paper.

2. FL – Ballast Frequency Response

Stable operation of LF in the wide range (3% to 100%) dimming applications can be obtained under the closed-loop control (Yin *et al.,* 2003). In the accordance with Deng (1996), the FL incremental impedance appears as a phase shift between the FL voltage envelope and the FL current one and can be modeled by the 1st order liner model. The model presents a pole on the left half-plane and a zero on the right half-plane and was analyzed in details in Ben-Yaakov *et al.* (2002). Analytical tools, proposed in Deng (1996), permit to derive a 6th order liner model for a 2nd order resonant filter and are useful for dynamic analysis of frequency-controlled DEB, however are very complex and not practical.

A practical approach to the stability analysis, used here, utilizes the frequency response of the DEB controlled in open-loop. The frequency response is obtained in the form of Bode graphs, the method widely adopted for linear systems analysis (Ogata, 2003). Although the FL is not a linear system, a linearization in turn of some operating point is possible. Figure 1 depicts the diagram used to obtain the Bode graphs, while Figure 2 shows the detailed implementation.

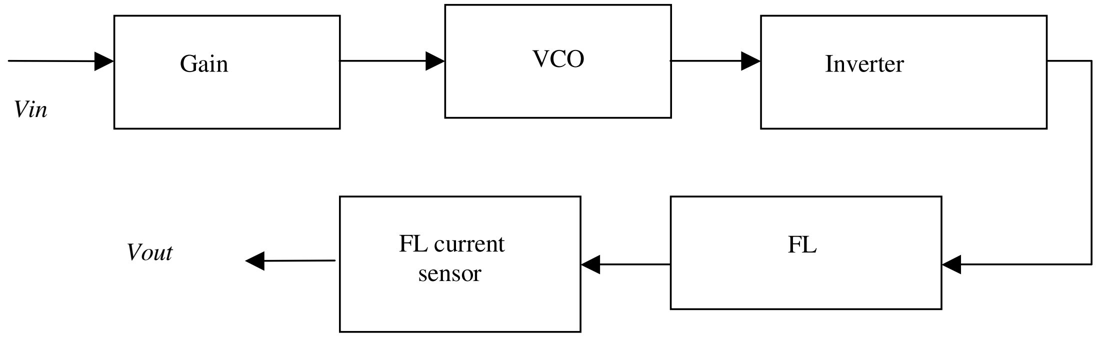


Figure 1: Diagram of the frequency response measuring.

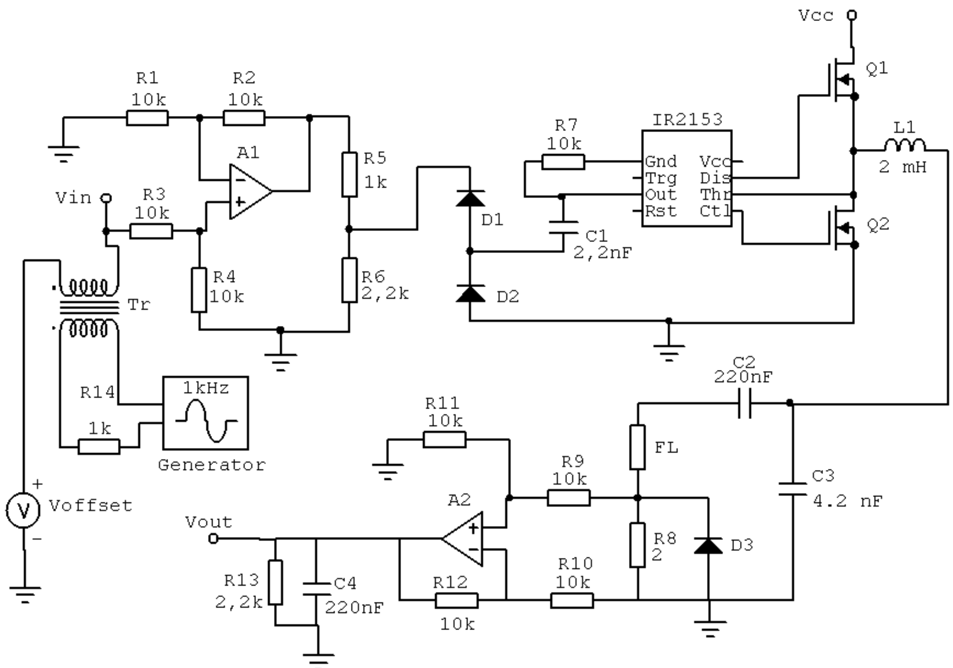


Figure 2: Implementation of the frequency response measuring.

The Vin(t) voltage is:

$$\mathrm{Vin(t)} = \mathrm{Voffset} + A \cdot \sin(2 \cdot \pi \cdot f_{MOD}) \qquad (1)$$

The magnitude of Voffset determines the dimming level of the FL, because the frequency on the VCO (*Voltage Controlled Oscillator*), implemented on the base of IR2153 integrated circuit, is proportional to the voltage on its input. The amplitude A of the modulation signal is adjustable and the modulation frequency, f_{MOD}, is varied. To obtain the frequency response, the FL power was adjusted to 7 W. Figure 3 shows Vin and Vout voltages measured on the prototype Figure 2 with Voffset= 0.56 V and f_{MOD}=100 Hz.

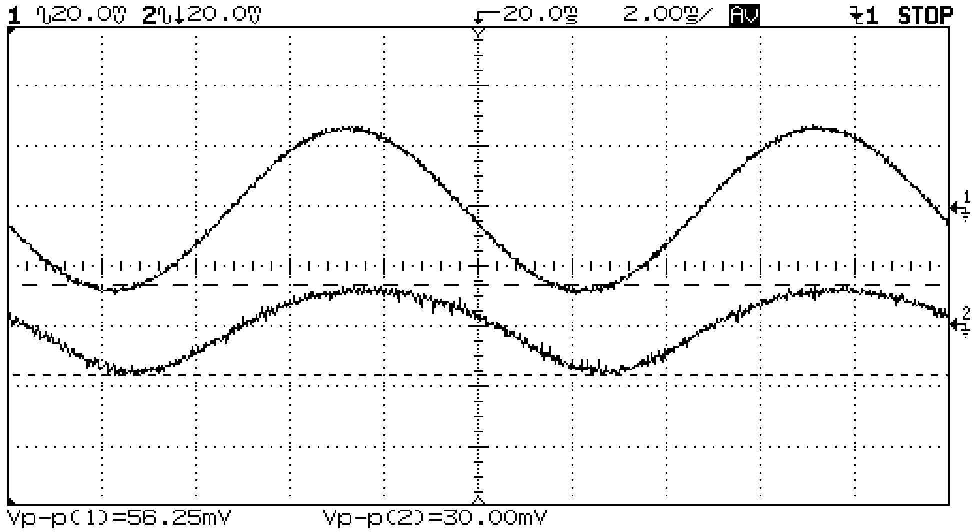
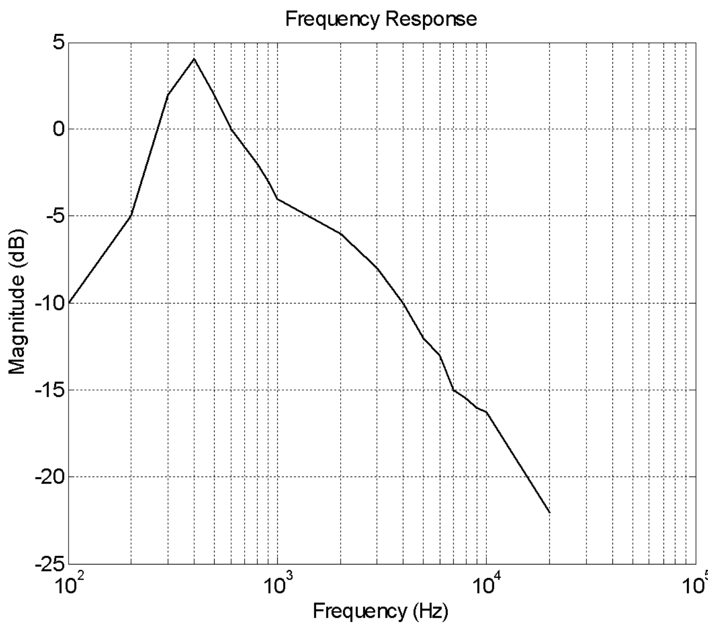
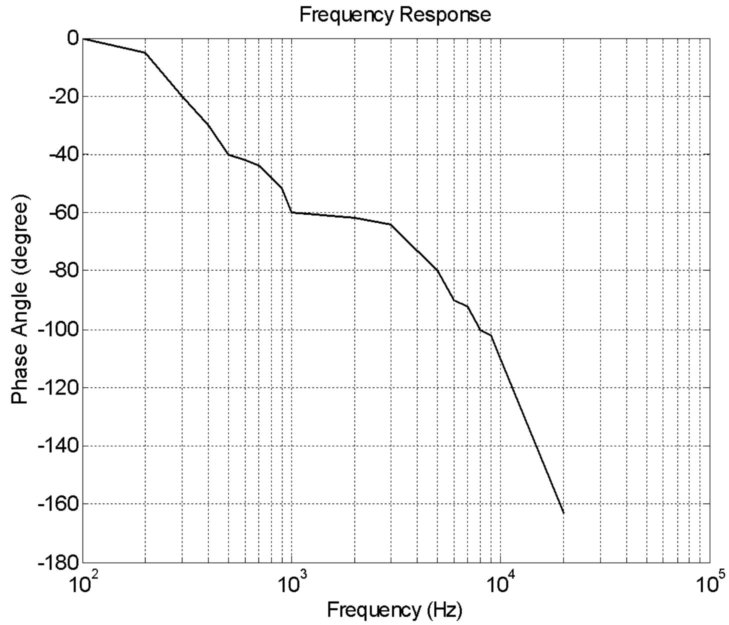


Figure 3 : Channel 1 – V_{in} (0,4 V/div); Channel 2 – V_{out} (0,4 V/div).

Figure 4 shows the Bode graphs obtained for TLD T8/32W model FL, Vcc=400 V; Voffset=2 V; resonant filter: L_1=2 mH; C2 = 220 nF; C1=4.2 nF. It should be noted that, when Voffset=2 V without modulating signal, the FL extinguishes.



a) $20 \cdot \log \left| \frac{Vout(s)}{Vin(s)} \right|$



b) $\arg\left(\frac{Vout(s)}{Vin(s)}\right)$

Figure 4: Frequency response measured on the open-loop controlled prototype.

3. Compensator Design

To achieve stable closed-loop operation, a DEB should include a compensator aiming sufficient gain and phase margins. A compensator should include one integrator to avoid stable-state error, thus way a PI compensator is a viable choice. Experiments proved that the gain crossover frequency of 7000 Hz is sufficient for stable arc control.

Observing Figure 4, one can conclude that the compensator corner frequency of about 1000 Hz guarantees a phase margin more than 50°. The gain margin should be above 6 dB. The following procedure is proposed for design the PI compensator:

1) $\omega_C = 1000 \cdot 2 \cdot \pi = 6280 \ \frac{rad}{s}$ (2)

where ω_C is the PI compensator's corner frequency.

2) The compensator gain should be equal to 15 dB at ω_C to guarantee the gain crossover frequency of 7000 Hz. This way, the compensator gain is:

$$20 \cdot \log_{10}\left(\frac{k}{\omega_C}\right) = 15\,\text{dB} \quad (3)$$

$$k = 10^{\frac{15}{20}} \cdot \omega_C = 35333 \quad (4)$$

3) Finally, the PI compensator transfer function is:

$$G_C(s) = k \cdot \frac{\left(\frac{1}{\omega_C} \cdot s + 1\right)}{s} = \frac{5.626 \cdot s + 35333}{s} \qquad (5)$$

The ballast with this compensator has the phase margin of 70^0 and gain margin of 7 dB.

The transfer function described by equation (5) can be easily implemented by one operational amplifier as shown in Figure 5.

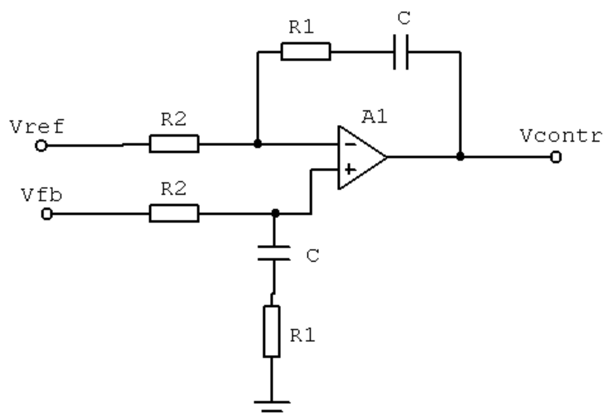


Figure 5: PI compensator implementation: C=5.1 nF; R1=31 kΩ; R2=5.6 kΩ.

4. Experimental Results

To verify the proposed design method, a DEB DIM_F prototype has been established on the base of IR2153 and LM324 operational amplifier to feed one TLD T8/32W model FL. The resonant filter has been implemented (Polonskii, 2005) as following: L_1 = 2 mH; C1 = 4.2 nF; C2 = 220 nF. A L6561-based PFC has supplied a 400 V DC bus. Figure 6 shows the designed ballast circuit except the PFC stage and the filament heating circuitry.

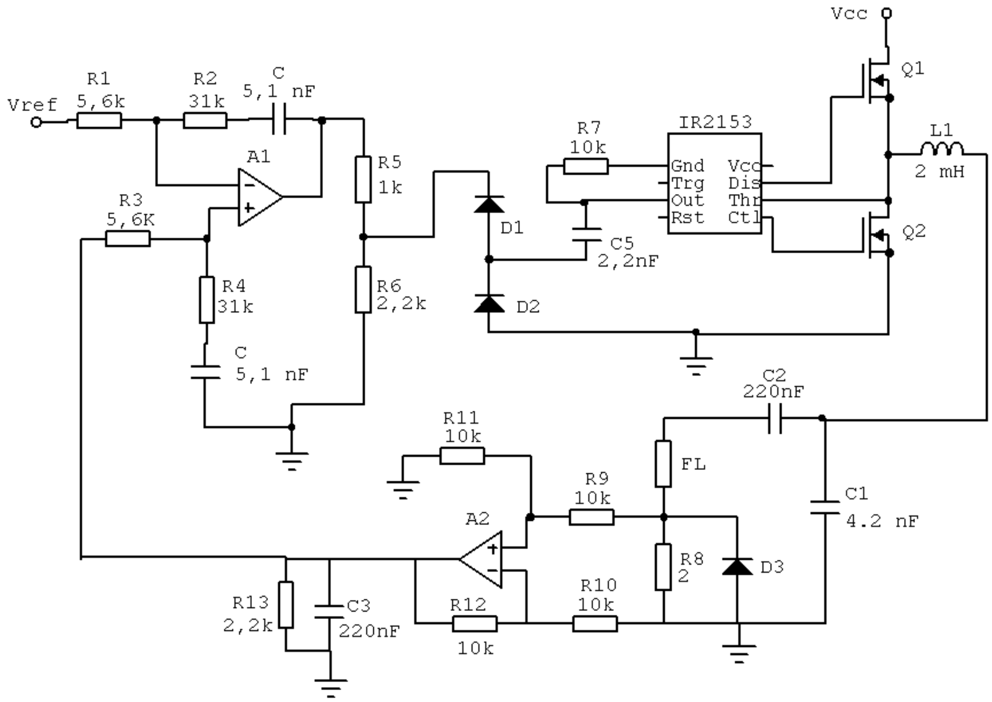
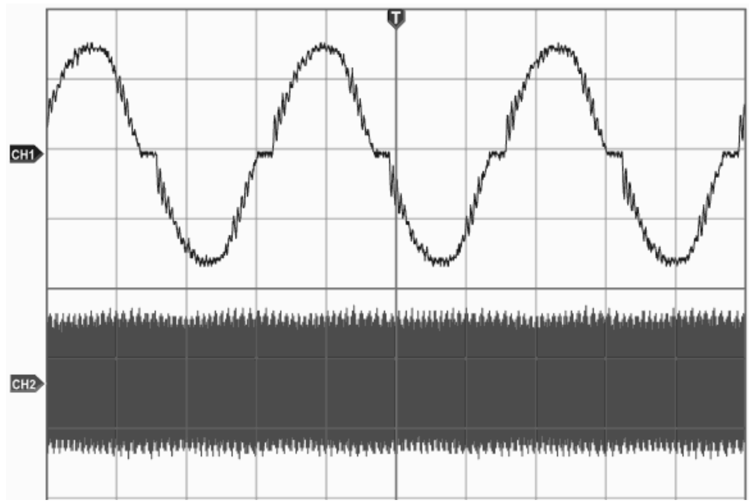


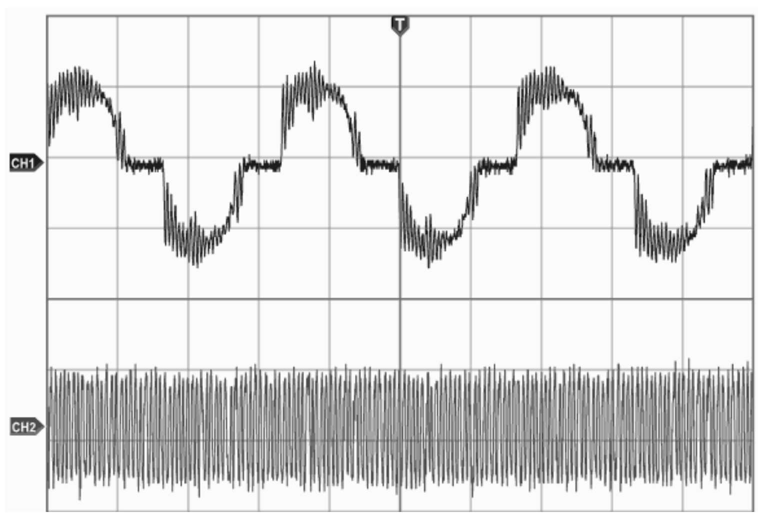
Figure 6: Designed ballast circuit.

It should be noted, that the reference signal (Vref in Figure 6), which is positive, is applied to the inverting input of the error amplifier A1, while the feedback signal enters into the non-inverting input. Although these polarities seem wrong, the circuit shown in Figure 6 is correct. The explication is that the half-bridge driver IR2153, which is controlled by the positive voltage on the A1 output, shifts to the higher switching frequencies when the A1 output voltage increases. The error amplifier A1 is a single supply operational one, so its output voltage is always positive. When the ballast circuit is turned-on, the positive Vref results in zero voltage on the A1 output and the switching frequency of IR2153 is the lowest one, defined basically by the values of C5 and R7. After the FL ignition, the feedback voltage begins to increase. When this voltage will be greater than the reference one, a positive voltage will appear on the A1 output, resulting in higher switching frequency and, consequently, in lower FL power. Being thus, it can be said that the designed ballast circuit includes some kind of additional virtual inverter, because when the error increases the output (FL power) decreases. Formally, dislocating this virtual inverter to the error amplifier input side, the signs of the reference and the feedback signals should be inverted, resulting in the commonly used polarities of the error amplifier inputs.

Figure 7 shows the input and FL currents measured on the prototype.



a) P=32 W; Superior - input current (0,2 A/div); Inferior – FL current (0,5 A/div)



b) P=1 W; Superior – input current (0,1 A/div); Inferior – FL current (0,05 A/div)

Figure 7: Experimentally measured currents.

Moreover, other dimming levels have been tested proving the stable prototype operation.

5. Conclusion

The paper presents a practical approach to design of wide dimming range DIM_F electronic ballasts. Closed-loop control permits a stable FL dimming until low power levels. A practical approach, which explores the open-loop system frequency response, permits to design a PI compensator for stable closed-loop operation. A DEB prototype, based on the proposed design method, operates stably while the FL is dimming till 3% of its rated power. Any attempt to dim the FL below 30% of its rated power under open-loop control results in arc distinguishing.

6. Acknowledgments

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